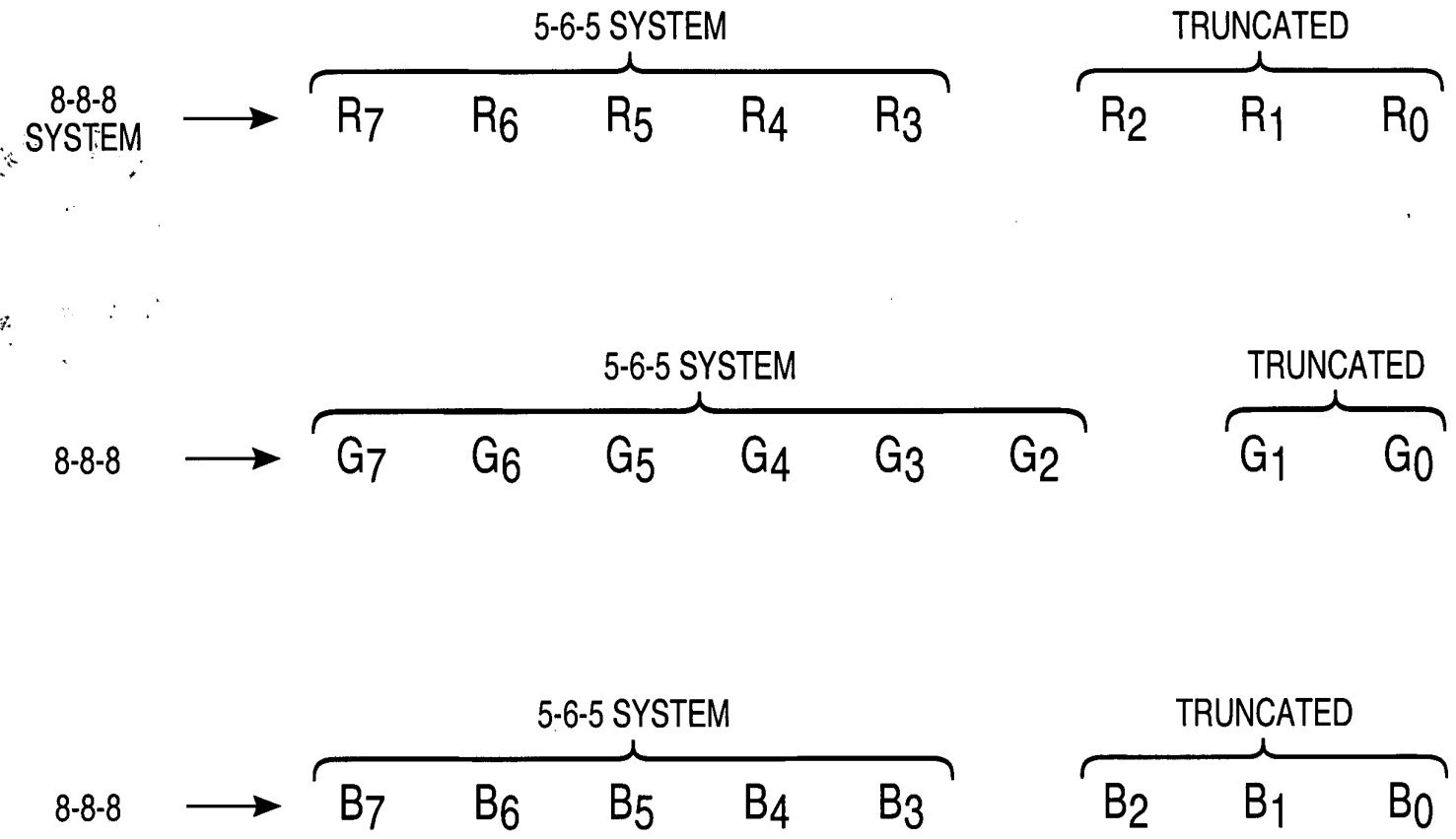
5-6-5 SYSTEM
TRUNCATED
8-8-8 SYSTEM
R7 R6 R5 R4 R3
R2 R1 R0
5-6-5 SYSTEM
TRUNCATED
8-8-8
G7 G6 G5 G4 G3 G2
G1 G0
5-6-5 SYSTEM
TRUNCATED
8-8-8
B7 B6 B5 B4 B3
B2 B1 B0

FIG. 1

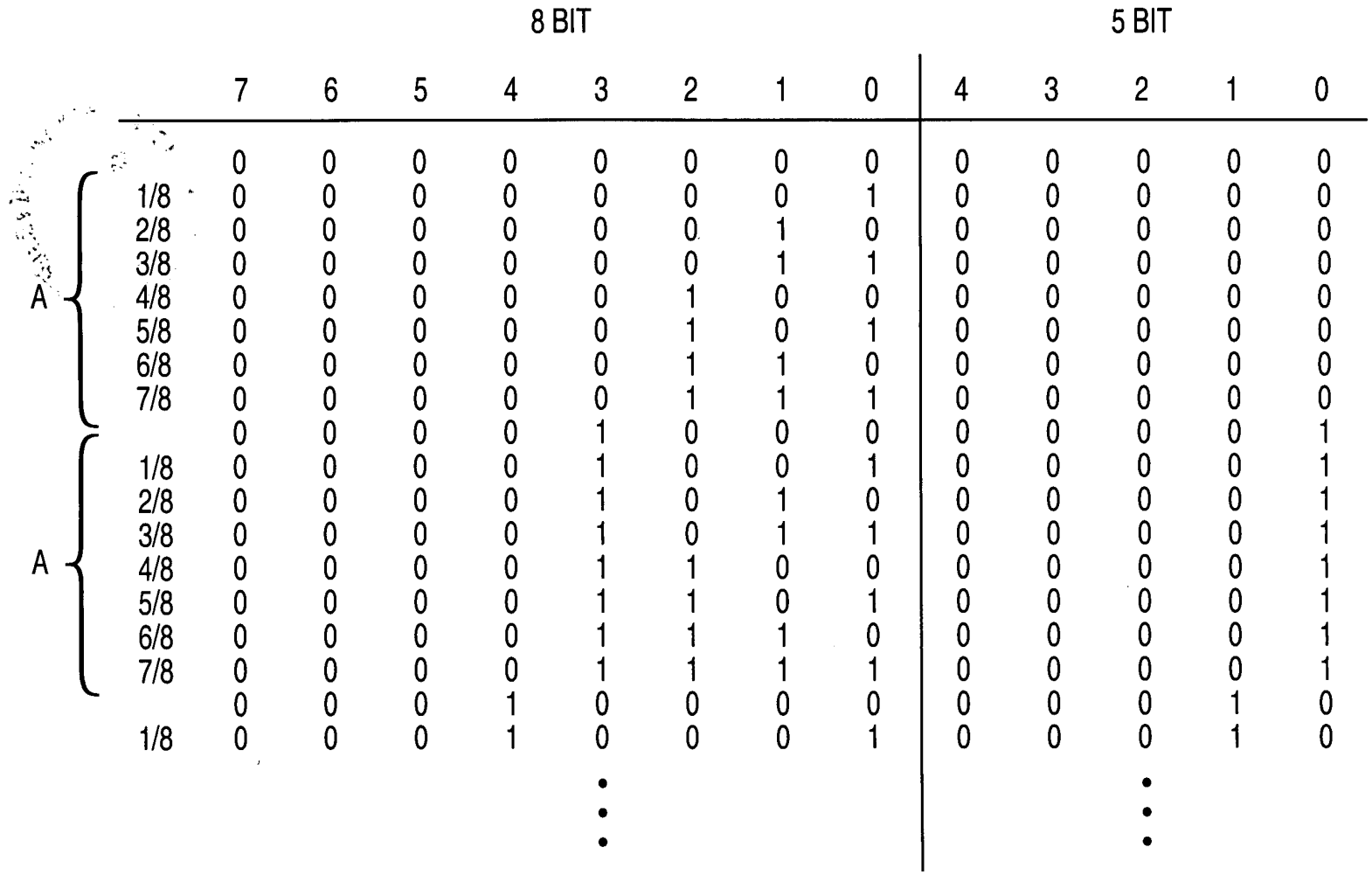
8 BIT
5 BIT
7 6 5 4 3 2 1 0 4 3 2 1 0
0 0 0 0 0 0 0 0 0 0 0 0 0
A
1/8 0 0 0 0 0 0 0 1 0 0 0 0 0
2/8 0 0 0 0 0 0 1 0 0 0 0 0 0
3/8 0 0 0 0 0 0 1 1 0 0 0 0 0
4/8 0 0 0 0 0 1 0 0 0 0 0 0 0
5/8 0 0 0 0 0 1 0 1 0 0 0 0 0
6/8 0 0 0 0 0 1 1 0 0 0 0 0 0
7/8 0 0 0 0 0 1 1 1 0 0 0 0 0
0 0 0 0 1 0 0 0 0 0 0 0 1
A
1/8 0 0 0 0 1 0 0 1 0 0 0 0 1
2/8 0 0 0 0 1 0 1 0 0 0 0 0 1
3/8 0 0 0 0 1 0 1 1 0 0 0 0 1
4/8 0 0 0 0 1 1 0 0 0 0 0 0 1
5/8 0 0 0 0 1 1 0 1 0 0 0 0 1
6/8 0 0 0 0 1 1 1 0 0 0 0 0 1
7/8 0 0 0 0 1 1 1 1 0 0 0 0 1
0 0 0 1 0 0 0 0 0 0 0 1 0
1/8 0 0 0 1 0 0 0 1 0 0 0 1 0

FIG. 2

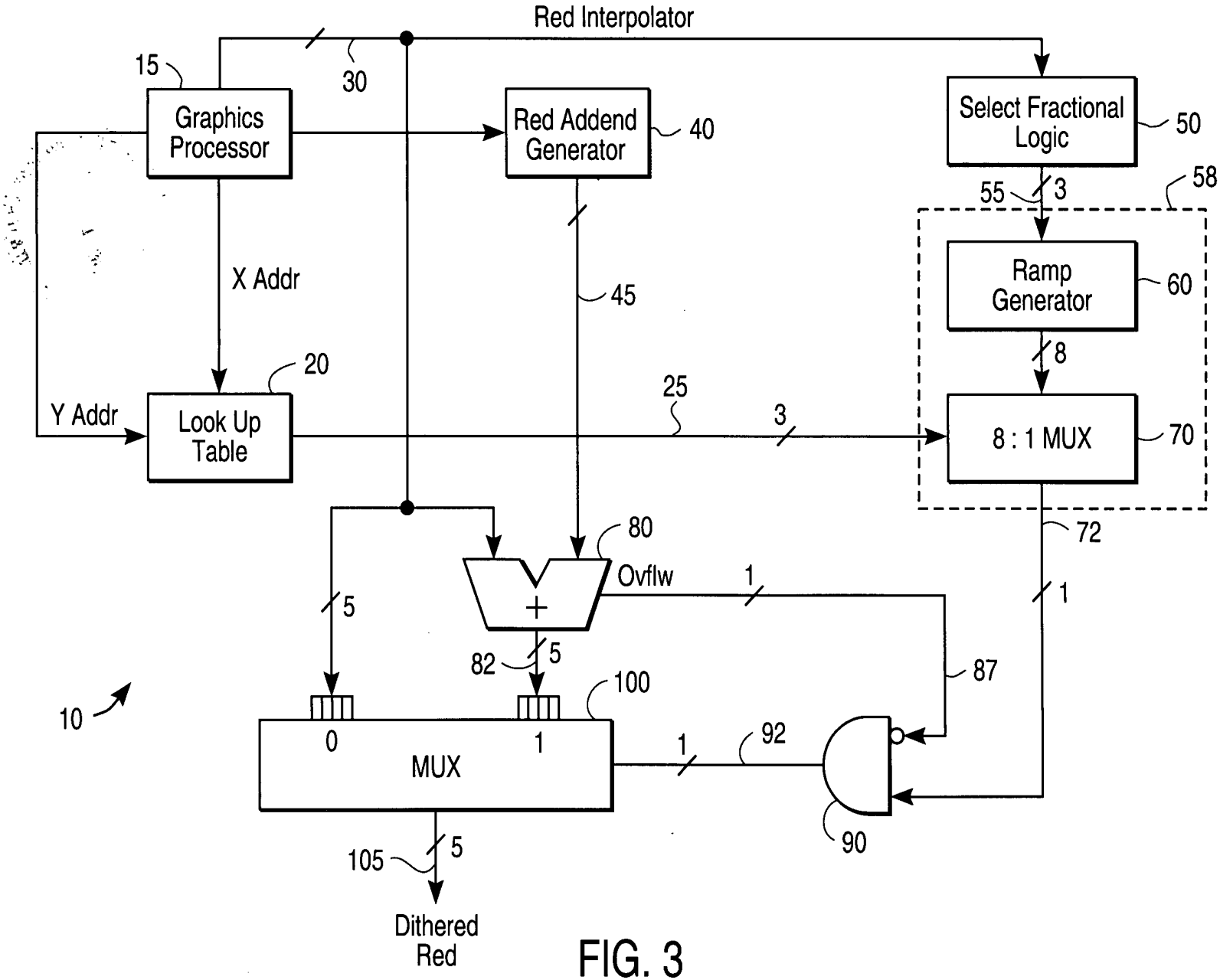
Red Interpolator
15
30
Graphics Processor
Red Addend Generator
40
Select Fractional Logic
50
55
3
58
X Addr
45
Ramp Generator
60
8
20
25
Y Addr
Look Up Table
3
8 : 1 MUX
70
80
72
Ovflw
1
5
1
82
5
87
100
10
0
1
MUX
1
92
90
105
5
Dithered Red

FIG. 3

		X Addr							
		0	1	2	3	4	5	6	7
Y Addr	0	0	4	1	5	0	4	1	5
	1	6	2	7	3	6	2	7	3
	2	1	5	0	4	1	5	0	4
	3	7	3	6	2	7	3	6	2
	4	0	4	1	5	0	4	1	5
	5	6	2	7	3	6	2	7	3
	6	1	5	0	4	1	5	0	4
	7	7	3	6	2	7	3	6	2

FIG. 4

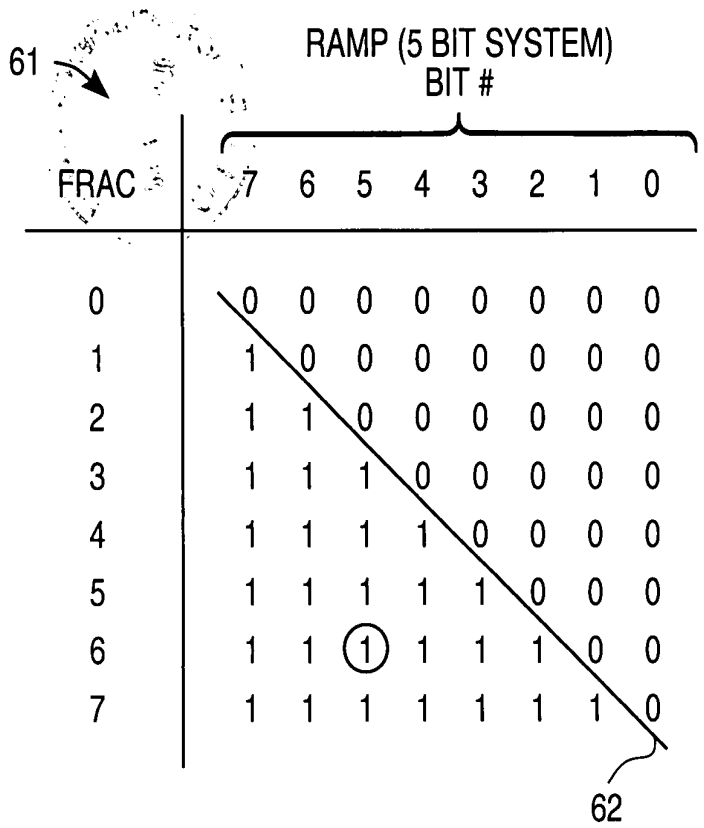
61
RAMP (5 BIT SYSTEM)
BIT #
FRAC
7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0
1 1 0 0 0 0 0 0
2 1 1 0 0 0 0 0
3 1 1 1 0 0 0 0
4 1 1 1 1 0 0 0
5 1 1 1 1 1 0 0
6 1 1 1 1 1 1 0 0
7 1 1 1 1 1 1 1 0
62

FIG. 5

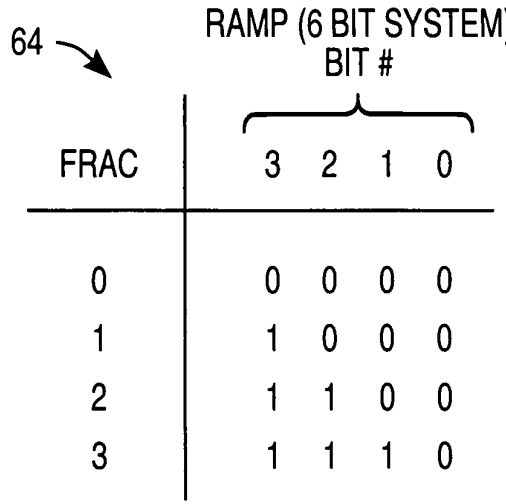
64
RAMP (6 BIT SYSTEM)
BIT #
FRAC
3 2 1 0
0 0 0 0 0
1 1 0 0 0
2 1 1 0 0
3 1 1 1 0

FIG. 6

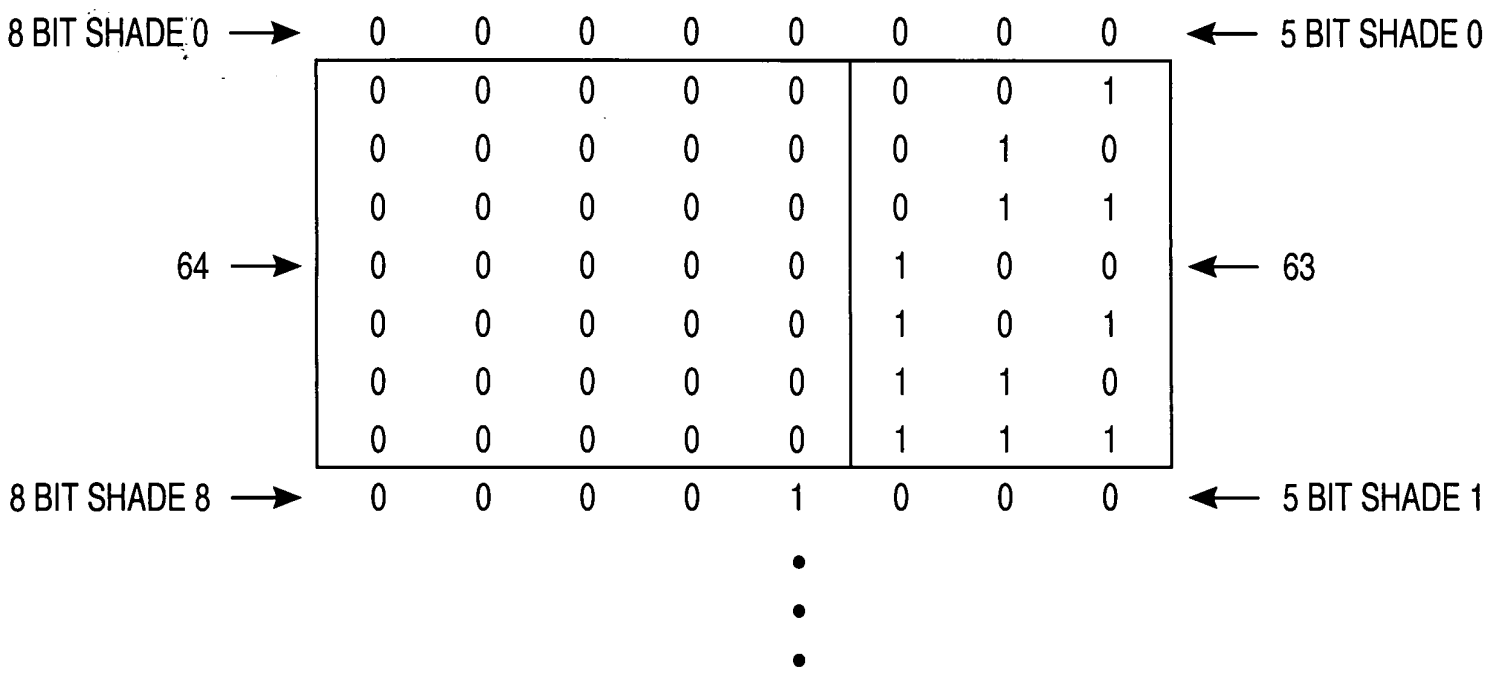
8 BIT SHADE 0
0 0 0 0 0 0 0 0
5 BIT SHADE 0
0 0 0 0 0 0 0 1
0 0 0 0 0 0 1 0
0 0 0 0 0 0 1 1
64
0 0 0 0 0 1 0 0
63
0 0 0 0 0 1 0 1
0 0 0 0 0 1 1 0
0 0 0 0 0 1 1 1
8 BIT SHADE 8
0 0 0 0 1 0 0 0
5 BIT SHADE 1

FIG. 7